Physical Oxide Thickness Extraction and Verification using Quantum Mechanical Simulation

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I. ABSTRACT

Physical gate oxide thickness is extracted from TiN gate PMOS and NMOS capacitance voltage measurements using an efficient multi-band Hartree self-consistent Poisson solver. The extracted oxide thicknesses are then used to perform direct tunneling current simulations. Excellent agreement between measured a simulated tunnel current is obtained without the use of adjustable fitting parameters.

II. INTRODUCTION

Sub-0.1um CMOS technologies require gate oxide thicknesses (t_{OX}) well below 30Å.[1] The success of TCAD tools in this regime depends in large part on the ability to quantitatively extract physical gate oxide thicknesses. One technique used to accomplish this is to utilize a Hartree self-consistent Poisson solver to match the MOS capacitance-voltage (CV) characteristic.[2,3] For oxide thicknesses below $\approx$ 20Å, capacitance measurements are difficult, if not impossible to perform due to large direct tunneling current. This implies that direct tunneling current (IV) simulation may be the preferred tool for physical $t_{OX} < 20$Å extraction. A required step to effectively use direct tunneling simulation in this capacity is to demonstrate that CV and IV extracted t_{OX} are in agreement. In previous work that compares CV and IV simulation physical material parameters (specifically the oxide effective mass) are used as adjustable fitting parameters to match tunneling simulation and experiment.[2] In this work we have fabricated, measured and simulated TiN gate NMOS *and* PMOS capicitors with thin gate oxide thicknesses ($\approx$ 20Å – 30Å). We perform t_{OX} extractions from CV characteristics using an efficient multi-band Hartree self-consistent Poisson solver. We then verify this extraction by comparing tunneling current simulation with measurement *without* the use of fitting parameters. This work suggests that it is possible to extract physical t_{OX} using tunnel current calculations provided that all of the relevant physics are included in the simulations.

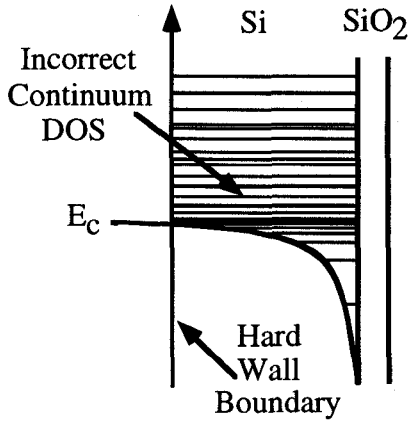

FIG. 1. Conduction band edge and eigenspectrum assuming a hard-wall boundary 20nm from the Si/SiO_2 interface. The silicon is doped n-type ($N_D = 2.0 \times 10^{17}$) and $2.0V$ is applied to the gate (accumulation). The density of states (DOS) in the energy continuum is significantly under-predicted using this boundary condition. In order to approximate the correct DOS one must move the hard-wall boundary far from the interface.

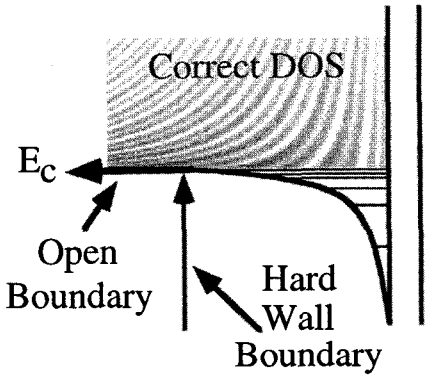

FIG. 2. Conduction band edge, bound state eigenspectrum and the continuum density of states for the same structure (and bias condition) shown in Figure 1. A hard-wall boundary condition is used to determine the bound eigenstates and an open boundary is used to calculate the density of states (DOS) in the continuum. Using these boundary conditions it is possible to calculate the correct accumulation charge using a small quantum mechanical simulation domain.

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III. CAPACITANCE SIMULATION

The Hartree Poisson solver used in this work is unique in that unphysical boundary conditions are not implemented. To our knowledge, all Hartree MOS simulators published in the literature impose a hard-wall boundary condition somewhere in the Si layer and calculate the entire energy eigenspectrum.[2–4] As illustrated in Figures 1 and 3 this boundary condition precludes one from calculating the correct density of states in the energy continuum unless a large simulation domain is used. In our simulator, the hard-wall condition is employed to calculate only the bound state spectrum.

As illustrated in Fig. 2 an open boundary condition is used to calculate the continuum density of states. This is important when one is calculating charge in accumulation layers since continuum states are within $\approx kT$ of the Fermi-level. Using our technique it is possible to obtain the correct charge distribution in accumulated layers using a small quantum simulation domain. This results in a speed performance of 60 capacitance bias points in less than 40 seconds on a standard workstation. In this work we employ a decoupled effective-mass bandstructure model that includes light and heavy holes ($m^*_{LH} = 0.16m_0; m^*_{HH} = 0.49m_0$) as well as longitudinal and transverse electrons ($m^*_t = 0.19m_0$; $m^*_l = 0.98m_0$).

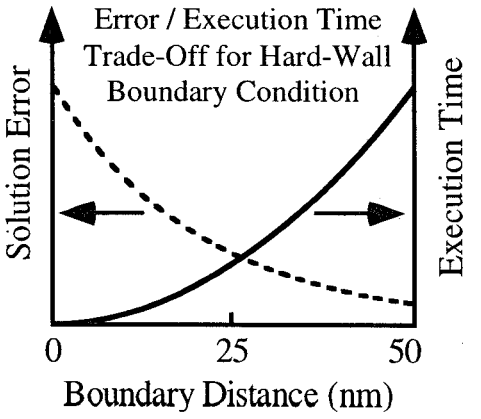

FIG. 3. Illustration of the Hartree-Poisson solution error and execution time vs. the hard-wall boundary distance from the Si/SiO_2 interface (i.e. quantum simulation domain size). Execution time increases with the square of the simulation domain while the solution error decreases asymptotically. Using our method it is possible to obtain a solution with zero intrinsic error using a small (< 25nm) quantum simulation domain.

IV. TUNNELING SIMULATION

The tunneling current calculations are carried out using a one-dimensional non-equilibrium Green's function simulator (NEMO) developed at Texas Instruments Inc.[5] A key feature of NEMO (see Fig. 4) is that it treats injection from quasi-bound states and continuum states on equal footing. Previous work on MOS tunneling assumes injection from either quasi-bound states[2] or a flat-band continuum.[6] Both of these assumptions are clearly incorrect for injection from accumulation layers. Moreover, the valence band must be included to correctly simulate tunneling from the valence band into the gate for biases above $\approx 1V$. Suprisingly, this effect has not been accounted for in the body of work on MOS tunneling.

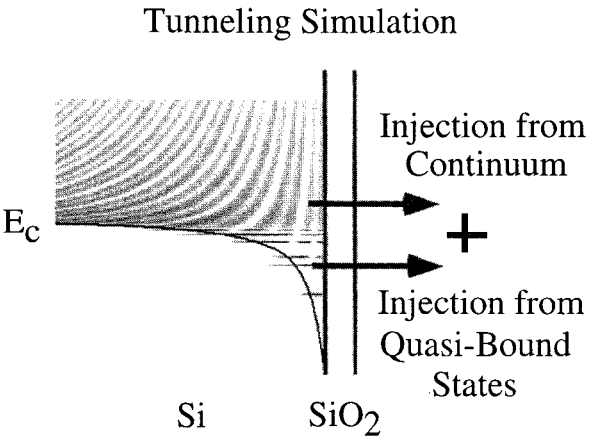

FIG. 4. Tunnel current is calculated using a non-equilibrium Greens function simulator that is capable of treating injection from quasi-bound states and continuum states on equal basis. Other work on MOS tunneling assumes that injection occurs from either quasi-bound states only or injection occurs from a flat-band (no band bending) continuum. Both of these assumptions do not predict the correct density of states in accumulated injection reservoirs.

In this work we employ a two-band $k \cdot p$ bandstructure model that incorporates both a valence and conduction band. Translational symmetry in the transverse direction dictates that transverse momentum be conserved. This selection rule has significant consequences for tunneling from negative curvature (i.e. valence) bands into positive curvature bands. As illustrated in Fig. 5, for a given value of transverse momentum in one dimension (eg. $k_y = 0$) tunneling is only allowed for a particular momentum ($k_x^{LEFT} = k_x^{RIGHT}$) and total energy

$E(k_x^{LEFT}, k_y = 0)$. Thus, in order to correctly simulate injection from valence band states it is necessary to numerically integrate over k_x and k_y. The relative magnitude of valence band injection current for a PMOS TiN gate capacitor is illustrated in Fig. 6. This is in general agreement with substrate current measurements on TiN gate NMOS devices (to be published).

V. RESULTS AND CONCLUSIONS

Standard optimization routines are employed to extract t_{OX} and gate workfunction using the Hartree Poisson CV simulator. For the thinner gate oxides we are not able to obtain reliable capacitance measurements in strong accumulation and inversion. Therefore, the objective function that is fed into the optimizer is defined only for biases which reliable measurements exist. The channel doping profile is obtained using SUPREM3.

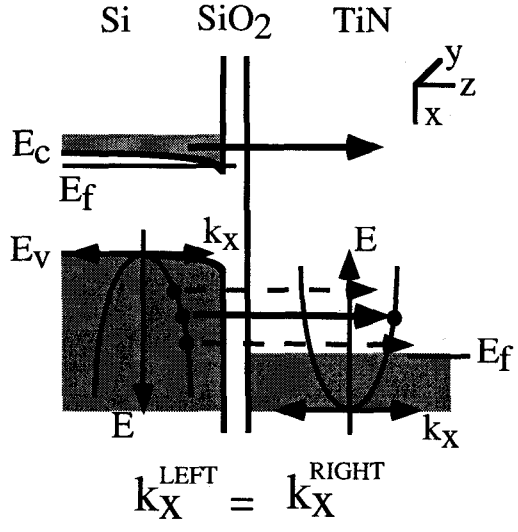

FIG. 5. Injection from valence band states into the gate occurs for gate biases higher than $\approx 1V$. In order to simulate this effect, a bandstructure model that includes coupled valence and conduction bands must be used. In this figure, $E - k_x$ diagrams (for $k_y = 0$) are shown for the Si valence band the the metal band. Translational invariance symmetry in the x and y directions dictates that tunneling can only occur if momentum in these dimensions is conserved. For $k_y = 0$, tunneling can occur for only one value of of k_x. The allowed transition is indicated by the solid arrow. Two unallowed transitions are indicated by dashed arrows. In order to obey this conservation rule one must numerically integrate over the momentum in the x and y dimensions.

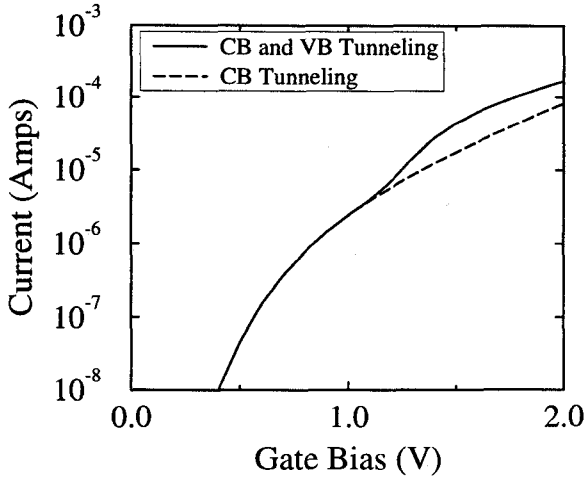

FIG. 6. Simulated PMOS capacitor tunnel current vs. gate bias with and without electron injectionf from the valence band. For gate biases above approximately 1V, current due to valence band injection becomes significant.

The oxide thicknesses extracted from the CV measurements are then used to perform tunnel current simulations. We stress that *no adjustable fitting parameters are implemented* in the tunneling simulations. The oxide effective mass ($m^*_{k\cdot p} = 0.42m_0$) has been independently determined.[7] The TiN effective mass is assumed to be m_0 and the density of states masses are implented in the Si layer.

Results are illustrated in Figs. 7-10 for both PMOS and NMOS capacitors. We obtain excellent agreement between simulated and measured tunneling current using the CV extracted oxide thicknesses. This suggests that the CV extracted oxide thicknesses are indeed physical and that thickness extraction from tunneling measurements may be feasable. The relative precision of CV and IV extracted t_{OX} is indicated in Figures 11 and 12.

We have demonstrated successful *physical* modeling (i.e. no adjustable fitting parameters) of tunneling in MOS structures. We believe this to be a critical milestone for the extraction of thin t_{OX} from tunneling current.

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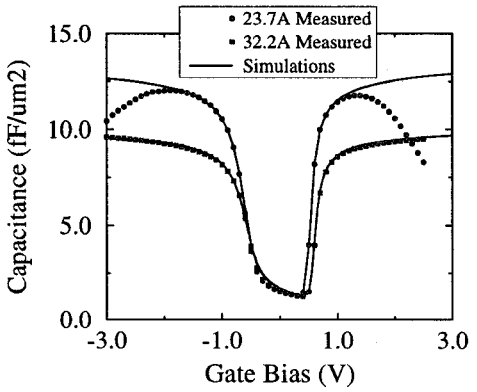

FIG. 7. Capacitance vs. voltage for TiN gate NMOS structures. The oxide thickness is extracted using a Hartree self-consistent Poisson solver by optimizing t_{ox} and gate workfunction to give the lowest root mean squared error. We are unable to obtain reliable capacitance measurements in strong inversion and accumulation for the sample with thinner oxide. For this structure we minimize the root mean squared error for biases between -1.0V and +1.0V.

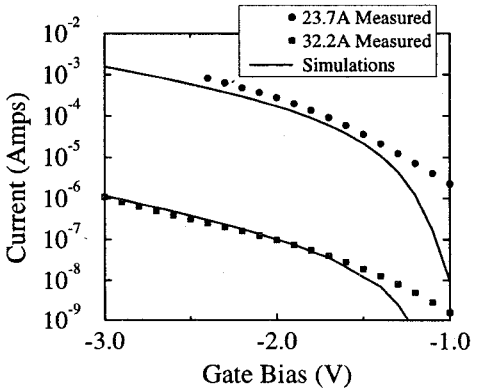

FIG. 8. Current vs. voltage corresponding to the capacitance measurements shown in FIG 7. The device area is $1.2x10^{-3}cm^2$. The oxide thickness extracted from the capacitance curves is used in the tunneling simulation. No adjustable fitting parameters are used in the tunneling simulations. The effective discrepancy between theory and experiment (at V_G=-2.0V) is 0.08A and 0.008A for oxide thicknesses of 23.7A and 32.2A respectively.

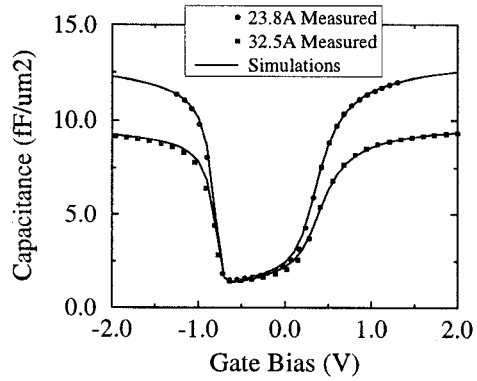

FIG. 9. Capacitance vs. voltage for TiN gate PMOS structures. The oxide thickness is extracted using a Hartree self-consistent Poisson solver by optimizing t_{ox} and gate workfunction to give the lowest root mean squared error. We are unable to obtain reliable capacitance measurements in strong inversion and accumulation for the sample with thinner oxide. For this structure we minimize the root mean squared error for biases between -1.2V and +1.2V.

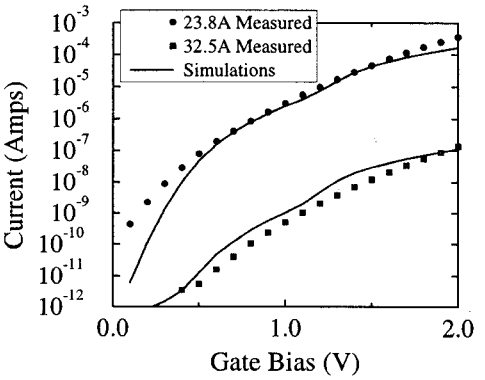

FIG. 10. Current vs. voltage corresponding to the capacitance measurements shown in FIG. 9. The device area is $1.2x10^{-3}cm^2$. The oxide thickness extracted from the capacitance curves is used in the tunneling simulation. No adjustable fitting parameters are used in the tunneling simulations. The effective discrepancy between theory and experiment (at V_G=1.0V) is 0.03A and 0.13A for oxide thicknesses of 23.8A and 32.5A respectively.

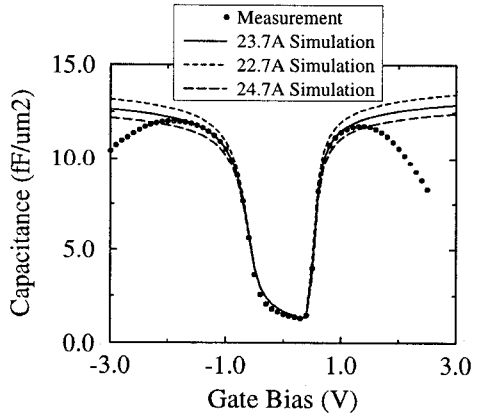

FIG. 11. Illustration of the sensitivity of the oxide thickness extraction using the CV characteristic.

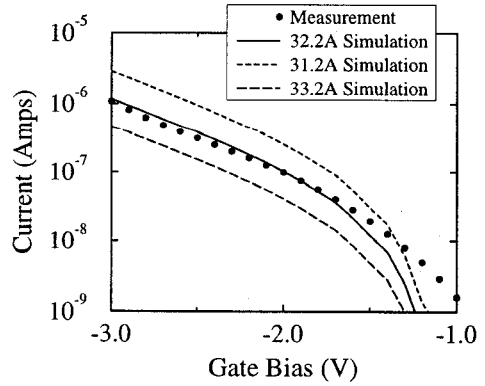

FIG. 12. Illustration of the sensitivity of the oxide thickness extraction using the IV characteristic.